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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,333	07/02/2002	Ilia Greenblat	56162.000371	8293

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HUNTON & WILLIAMS LLP
INTELLECTUAL PROPERTY DEPARTMENT
1900 K STREET, N.W.
SUITE 1200
WASHINGTON, DC 20006-1109

EXAMINER	
FERRIS, DERRICK W	

ART UNIT	PAPER NUMBER
2663	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,333	GREENBLAT ET AL.	
	Examiner	Art Unit	
	Derrick W. Ferris	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1-7 and 9-11** are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,886,992 A to *Raatikainen et al.* ("*Raatikainen*").

As to **claim 1**, see e.g., figure 1 which shows a plurality of ring members as nodes (e.g., 102, 104) on a ring that communicate using point-to-point connectivity (i.e., each node is connected to one another as shown in the figure), see e.g., column 9, lines 10-26. As to e.g., a message traversing the ring from member to member, the data is transmitted from node to node by using slots, see e.g., column 10, lines 10-19. As to the system being adapted so that upon the message arriving at a given ring member the message is processed by that ring member if the message is applicable to that ring member, if the message is not applicable to that ring member, the message is passed on to the next ring member, see e.g., column 11, lines 44-50 where the node contains control logic that decides when to transmit and receive data on the ring. As to means for providing an external ring interface enables communication with at least one external peripheral

device, see e.g., figure 2 with respect to peripheral input and output. In addition, see e.g., column 9, lines 40-51 with respect to a peripheral interface.

As to **claim 2**, see e.g., column 18, lines 16-54 with respect to FPGA.

As to **claim 3**, see e.g., figure 2 which shows a "memory port" as e.g., the peripheral transmit and receive buffers 122, see also column 16, lines 44-59.

As to **claims 4-6**, the node control processor 118 performs protocol conversion, thus teaching a reasonable but broad interpretation of handshaking in view of converting messages, see e.g., column 9, lines 40-52.

As to **claim 7**, see e.g., figure 2 which shows a "shared memory" as e.g., the peripheral transmit and receive buffers 122, see also column 16, lines 44-59. In particular, the memory is considered shared since it is between the peripheral and the ringed network.

As to **claim 9**, see e.g., column 15, lines 57-65 where the external device is e.g., a second ringed network and the peripheral bus is the external bus.

As to **claim 10**, see e.g., column 15, lines 57-65 where the external device is e.g., a second ringed network such that the nodes are able to communicate with other ring networks such as the disclosed ringed network where each ring network is on a chip.

As to **claim 11**, see similar rejection to claim 10. In particular, see e.g., figure 2 with respect to a first protocol processor and a second protocol processor 118 (i.e., each node has at least one protocol processor).

3. **Claims 1 and 3-9** are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,687,757 B1 to *Ben-Ze'ev et al.* ("*Ben-Ze'ev*").

As to **claim 1**, see e.g., figures 3, 4, or 6 which shows a plurality of ring members as e.g., processors on a ring that communicate using point-to-point connectivity. In particular, note that the reference teaches two rings, a tubular bus 29 and a ring bus 44 (management bus), both which have nodes such as a host processor 26 which are connected in a point-to-point fashion thus meeting the claim limitation. As to e.g., a message traversing the ring from member to member, the data is transmitted from node to node by using slots, see e.g., column 6, line 64 – column 7, lines 53 with respect to transmitting data on the bus/ring. As to the system being adapted so that upon the message arriving at a given ring member the message is processed by that ring member if the message is applicable to that ring member, if the message is not applicable to that ring member, the message is passed on to the next ring member, see e.g., column 6, line 64 – column 7, lines 53 and more specifically column 9, lines 1-35 and column 14, lines 27-54 with respect to an address filter 82,84. As to means for providing an external ring interface enables communication with at least one external peripheral device, see e.g., figure 3 with respect to the PCI interface 25 that interfaces with a peripheral device such as host 26. See also external interface 66 which also interfaces with external devices on the network.

As to **claim 3**, with respect to a "memory port' see e.g., figure 3 which teaches FIFO 61, 62 and DMA 27.

As to **claim 4-6**, see e.g., column 7, lines 1-52 with respect to deframing the data in order to place the data on the bus. Thus the data is converted using a handshaking method. Also note that the data is further sent/received from the bus.

As to **claim 7**, with respect to a "shared memory see e.g., figure 3 which teaches FIFO 61, 62 and DMA 27.

As to **claim 8**, see e.g., FIFO 61, 62 in figure 3. Also each packet processor has dual-port RAM, see e.g., column 10, lines 1-55.

As to **claim 9**, see e.g., bus 25 which is an external bus.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,687,757 B1 to *Ben-Ze'ev et al.* ("*Ben-Ze'ev*") in view of "Alternative approach to ASIC design methodology based on reconfigurable logic devices" to *Dunlop et al.* ("*Dunlop*").

As such to **claim 2**, *Ben-Ze'ev* discloses a Field Programmable Processor Array (FPAA), see e.g., column 5, lines 60-61 but does not specifically teach a FPGA.

Dunlop teaches the further recited limitation above at e.g., right-hand column on page 217

The proposed modification of the above-applied reference(s) necessary to arrive at the claimed subject matter would be to modify *Ben-Ze'ev* by clarifying that using FPGA as a design choice are well known in the prior art.

As such, examiner notes that it would have been obvious to one skilled in the art prior to applicant's invention to include the above limitation. In particular, the motivation

for modifying the reference or to combine the reference teachings would be to configure and reconfigure a device an unlimited number of times. In addition, a further motivation is a matter of hardware design choice. In particular, *Dunlop* cures the above-cited deficiency by providing the above motivation found at e.g., right-hand column on page 217.

6. **Claim 12** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,687,757 B1 to *Ben-Ze'ev et al.* ("*Ben-Ze'ev*") in view of U.S. Patent No. 5,822,586 A to *Swanstrom*.

As such to **claim 12**, *Ben-Ze'ev* is silent or deficient to wherein the ring network can write data to an address in the memory to cause an interrupt in the at least one external peripheral device.

Swanstrom teaches the further recited limitation above at e.g., Abstract.

The proposed modification of the above-applied reference(s) necessary to arrive at the claimed subject matter would be to modify *Ben-Ze'ev* by clarifying that the ring network can write data to an address in the memory to cause an interrupt in the at least one external peripheral device is well known in the art prior to applicants invention.

As such, examiner notes that it would have been obvious to one skilled in the art prior to applicant's invention to include the above limitation. In particular, the motivation for modifying the reference or to combine the reference teachings would be to inform the external peripheral on the status of reading/writing information to memory. In particular, *Swanstrom* cures the above-cited deficiency in the Abstract.

7. **Claim 12** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,886,992 A to *Raatikainen et al.* ("*Raatikainen*") in view of U.S. Patent No. 5,822,586 A to *Swanstrom*.

As such to **claim 12**, *Raatikainen* is silent or deficient to wherein the ring network can write data to an address in the memory to cause an interrupt in the at least one external peripheral device.

Swanstrom teaches the further recited limitation above at e.g., Abstract.

The proposed modification of the above-applied reference(s) necessary to arrive at the claimed subject matter would be to modify *Raatikainen* by clarifying that the ring network can write data to an address in the memory to cause an interrupt in the at least one external peripheral device is well known in the art prior to applicants invention.

As such, examiner notes that it would have been obvious to one skilled in the art prior to applicant's invention to include the above limitation. In particular, the motivation for modifying the reference or to combine the reference teachings would be to inform the external peripheral on the status of reading/writing information to memory. In particular, *Swanstrom* cures the above-cited deficiency in the Abstract.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Derrick W. Ferris whose telephone number is (571) 272-3123. The examiner can normally be reached on M-F 9 A.M. - 4:30 P.M. E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571)272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Derrick W. Ferris
Examiner
Art Unit 2663

DWF

1/31/06
DERRICK FERRIS
PATENT EXAMINER